Investigation of the hot carrier degradation in power LDMOS transistors with customized thick oxide

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Abstract

In this paper, we report a combined experimental/simulation analysis of the degradation induced by hot carrier mechanisms, under ON-state stress, in silicon-based LDMOS transistors. In particular, the ON-resistance degradation in linear regime has been experimentally characterized by means of different stress conditions and temperatures. The hot-carrier stress regime has been fully reproduced in the frame of TCAD simulations by using physics-based models able to provide the degradation kinetics. A thorough investigation of the spatial interface trap distribution and its gate-bias and temperature dependences has been carried out achieving a quantitative understanding of the degradation effects in the device.

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1. Introduction

Nowadays, the lateral double-diffused MOS (LDMOS) power transistor represents device of choice for smart power technologies because of its compatibility with CMOS technology [1, 2]. However, because of the complex lateral structure, the high fields at the silicon/oxide interface intensify the degradation mechanisms affecting the device reliability. In particular, when the device operates in ON-state regime, electrons can gain sufficient kinetic energy (hot carriers) necessary to create interface states followed by charge trapping causing the reduction of the device performance [3].

Being one of the most critical issues affecting the LDMOS reliability [3], various predictive models have been recently developed based on analytical relationships or suitable for TCAD investigations [4-6]. In [7], by taking into account the interaction of the hot carriers with interface molecules and the thermal-field interaction with the lattice, the hot carrier degradation has been nicely predicted for an extended range of stress conditions and device geometries by using a TCAD tool. However, the LDMOS devices investigated in the previous works are mainly focused on architectures with a shallow-trench isolation (STI) since they are known to lead significant benefits in reducing chip size even if worsening $R_{ON}$ degradation during reliability tests because of the high electric field occurring at the STI edges [8].

In this paper, a hot carrier degradation analysis has been performed on medium rated voltage N-drift LDMOS transistors with customized thick oxide aimed at optimizing the SOA limitations coming from the STI architecture [9]. In particular, the ON-resistance degradation in linear regime has been experimentally investigated for an extended range of stress conditions and nicely reproduced by means of TCAD simulator. Consequently, the spatial interface trap distribution has been evaluated and its gate bias dependence has been investigated.

2. Device Structure, Experimental Setup and TCAD Calibration

Medium rated voltage N-drift LDMOS transistors, fabricated on 200mm-wafers by STMicroelectronics [9], are considered and shown in Fig. 1.

The devices under investigation feature a customized thick oxide in the N-drift region aimed at optimizing the SOA limitations of STI architecture [9]. In order to investigate the device degradation due to hot carrier stress (HCS) and to spatially localize the

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interface trapped charge, experimental analyses combined with TCAD simulations have been performed.

The device degradation has been experimentally carried out on-wafer by adopting the conventional measure/stress/measure technique. Consequently, HCS induced degradation is evaluated by monitoring the \( R_{\text{ON}} \) shift in linear regime.

Finally, the simulated structure has been defined and calibrated in the frame of the Sentaurus TCAD simulator [10] considering the geometric characteristics and the material properties of the devices under test (DUT). In particular, process simulations have used to define the doping profiles, a slight change to the gate barrier has been applied and a fine tuning of the low-field mobility dependence on the normal electric field has been carried out in order to obtain the nice agreement between experimental and simulated \( I_DV_G \) transfer characteristics as shown in Fig. 2.

Moreover, in order to correctly reproduce the HCS conditions in ON-state, the heat transfer equation has been used and thermal resistances have been added at the contacts and calibrated against measured output characteristics in order to reproduce the self-heating effects in the device. Then, the VanOverstraeten impact-ionization model has been turned on with default parameter values allowing for a nice prediction of the avalanche regime onset at larger \( V_{\text{DS}} \) (Fig.3).

3. Results and Discussion

In order to understand which are the worst HCS conditions, the body current has been monitored because of its correlation with the impact ionization generation and hence with the number of carriers gaining enough energy to eventually generate interface traps. Fig. 4 shows the simulated body current (a) with the corresponding impact ionization generation term (b). The higher the impact ionization peak the higher the absolute body current. Moreover, the body-current characteristics reveal a strong increase of impact ionization with a first peak at \( V_{\text{GS}} \) about 1.9 V, which is usually adopted as a worst-case condition for the HCS investigations. This initial rise is attributed to the steep increase of the channel current in the near-threshold regime, with carriers experiencing a region of high electric field close to the channel. By increasing the gate bias the impact ionization peak moves toward the drain (Fig. 4b) and the body current rises again to larger values due to the Kirk effect at the drain edge.

It is worth noting that it was not possible to experimentally monitor the body current because body
and source contacts are internally short-circuited in the real device.

By considering the simulated body current in Fig. 4a, three different stress conditions have been chosen in order to verify the correlation between impact ionization (hot carrier) and device HCS degradation. In Fig. 5, the ON-resistance degradation extracted in linear regime for the three selected stress conditions is reported, showing a nice correlation with the simulated body current (Fig. 4a).

In general, the large electric fields causing HCS damage are strongly localized in well-defined regions as shown by Fig. 4b. In order to simulate the $R_{\text{ON}}$ degradation, the HCS degradation model proposed in [7] has been adopted along with numerical solution of the Boltzmann transport equation implemented in [10]. However, since the HCS model was previously used for STI-LDMOS transistors, a first calibration procedure has been carried out on the structure under analysis. To this purpose, as for stress conditions at low $V_{\text{GS}}$ the major role is played by the single-electron hot-carrier processes, the corresponding model has been incorporated first and the parameters have been calibrated on the $\Delta R_{\text{ON}}$ experiments. More specifically, the maximum number of interface bonds and the fitting constant in the reaction cross-section have been slightly tuned against experiments. The HCS model has been finally carried out at different gate biases, showing a very nice agreement with experiments (Fig. 5) confirming that the single-electron HCS process is the most relevant one for this kind of devices. No relevant threshold voltage shift has been experimentally observed under stress, thus indicating no degradation localized in the channel region at large gate biases. Moreover, the maximum temperature due to self-heating has been monitored showing values below the threshold of the thermal degradation.

Fig. 6 shows the interface trap creation during the stress in the case of $V_{\text{GS}} = 1.9$ V (a) and $V_{\text{GS}} = 4.8$ V (b) with $V_{\text{DS}} = 18$ V and $T = 25$ °C. It is possible to note that: i) a huge interface trap creation occurs close to drain contact (cut 1, Fig. 1) independently of the applied gate bias. However, since the region below/around the drain contact is highly doped (not shown) in order to reduce the contact resistance, $R_{\text{ON}}$ is insensitive to interface charge trapped in this region; ii) by observing cuts 3 and 4, the interface trap responsible for the $R_{\text{ON}}$ degradation at low $V_{\text{GS}}$ is created in the region of the thick oxide (selective epitaxial growth) showing a strong localization.
LOCOS; iii) by increasing the gate bias (VGS = 4.8 V) the trap creation moves toward the drain contact (cut 2, Fig 6b). This is well appreciable in Fig. 7 where the interface trapped charge is shown after 2·10^3 s of stress at VGS = 1.9 V (a) and VGS = 4.8 V (b), VDS = 18 V and T = 25 °C. The gate bias dependence of the spatial interface trap distribution is in agreement with the localized impact ionization peak shown in Fig. 4b. By increasing the gate bias the impact ionization peak, hence the region where electron feature high kinetic energy, moves toward the drain creating defects at the silicon/oxide interface (Fig. 6).

Finally, in order to further validate the correct implementation of the HCS model, the device degradation has been characterized at different stress temperatures. Fig 8 shows the ON-resistance degradation as a function of ambient temperature, both experiments (symbols, Fig. 8a) and simulation data (lines, Fig. 8) are reported. As expected for the single-electron hot-carrier process, by increasing the temperature during the stress, the ΔRON is reduced because of the phonon increase: the electron-phonon interactions tend to redistribute electrons from the high-energy tail to lower energies, thus reducing the HCS processes. As the HCS model in [7] accounted for the physical dependence on temperature, a nice agreement with experiments has been obtained.

3. Conclusions

In this work, we investigated the hot carrier degradation in medium rated voltage N-drift LDMOS transistors with a customized thick oxide instead of the conventional shallow-trench isolation one.

In particular, the HCS degradation has been experimentally characterized by means of different stress conditions. Then, by exploiting a preliminary device calibration, the ON-resistance degradation induced by HCS has been fully reproduced by TCAD simulations for an extended range of voltages and temperatures. Thanks to this approach, the charge trapping responsible for the RON degradation has been identified and spatially localized at the silicon/oxide interface of the selective LOCOS.

Finally, the TCAD analysis has been validated against experiments up to 100 °C.

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References